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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,196	08/26/2003	Huan-Ping Su	MM4635	6273
7590 06/03/2005 ANDERSON KILL & OLICK, P.C. 1251 Avenue of the Americas New York, NY 10020			EXAMINER NADAV, ORI	
			ART UNIT 2811	PAPER NUMBER
DATE MAILED: 06/03/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

**Office Action Summary**

Application No.

10/650,196

Applicant(s)

SU, HUAN-PING

Examiner

ori nadav

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**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 April 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky (5,280,192) in view of Heo (6,555,917), Farnworth et al. (6,501,165) and Applicant Admitted Prior Art (AAPA).

Kryzaniwsky teaches in figure 4 and related text a flip chip semiconductor package, comprising:

a first chip carrier substrate 12 mounted with at least a first chip 5 having a first active and non-active surfaces opposite each other wherein a plurality of first inner leads 20, 21 are formed on the first active surface in direct contact with the first chip carrier for electrically connecting the first chip to the first chip carrier;

a second chip carrier substrate 13 mounted with at least a second chip 6 having a second active and non active surfaces opposite each other wherein a plurality of second inner leads are formed on the second active surface in direct contact with the first chip carrier for electrically connecting the second chip to the second chip carrier;

the first non active surface of the first chip is attached to second non active surface of the second chip;

a resin encapsulating layer (11 and the resin covering leads 20, 21) filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the first and second inner leads; and

a plurality of conductive vias 14, 15 penetrating the first chip carrier 12, the resin encapsulating layer 11 and the second chip carrier 13 so that the second chip carrier forms a direct electrical connection to the first chip carrier via the conductive vias. Kryzaniwsky does not teach using solder bumps and an adhesive layer to attach the second chip to the first chip.

Heo teaches in figure 8A and related text using an adhesive layer 28 to attach the second chip 10-3 to the first chip 10-2.

Farnworth et al. teach in figures 5A and 5D and related text a plurality of solder balls 76A formed on the first active surface in direct contact with the first chip carrier 14A for electrically connecting the first chip to the first chip carrier 22A.

AAPA teaches on page 3 the advantages of using solder balls instead of inner leads.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use solder bumps instead of inner leads and an adhesive layer to attach the second chip to the first chip in Kryzaniwsky's device, in order to improve the reliability of the device and to provide better bonding between the two chips, respectively. The combination is motivated by the teachings of AAPA which points out the advantages of using solder balls (page 3).

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Regarding claim 2, Farnworth et al. teach in figure 5A a plurality of solder bumps disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

Regarding claims 4 and 9, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tape carrier in prior art's device in order to use the device in an application which requires a tape carrier.

Regarding claims 5 and 10, Heo teaches in figure 8A an adhesive layer 28 being an insulating adhesive having high elasticity.

Regarding claims 6 and 11, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a resin encapsulating layer being made of resin materials having low hygroscopicity and low viscosity in prior art's device in order to improve the protection for the device.

Regarding claim 7, Kryzaniwsky teaches in figure 4 and related text a plurality of conductive traces 14, 15 formed over the first chip carrier, the resin encapsulating layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via each of the conductive traces.

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Regarding claim 12, Kryzaniwsky teaches conductive traces have one end connected to the ball pads of the second chip carrier and the other end connected to the ball pads 152 of the first chip carrier.

Regarding claims 13-16, the device of prior art includes conductive vias comprising a plurality of through holes opening through the first chip carrier, the resin encapsulating layer, and the second chip carrier, wherein a conductive layer is formed on an inner wall of each of the through holes to define a cavity, wherein the conductive layer is made of a copper foil, wherein the cavity is filled by a conductive material.

Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kryzaniwsky, Heo, Farnworth et al. and AAPA, as applied to claims 1, 7, 13 and 14 above, and further in view of Kim (5,407,864).

Kryzaniwsky, Heo, Farnworth et al. and AAPA teach substantially the entire claimed structure, as recited in claims 1, 7, 13 and 14 above, except a cavity filled by a dielectric material, and a dielectric solder mask for encapsulating the conductive traces.

Kim teaches in figure 2F a cavity 9 filled by a dielectric material 14, and a dielectric solder mask for encapsulating the conductive traces 12.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to fill the cavity in prior art's device by a dielectric material, wherein a dielectric solder mask encapsulating the conductive traces, in order to provide high

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density method of mounting semiconductor chips with enhanced manufacturing characteristics.

***Response to Arguments***

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

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Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**.

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized flourish at the end.

O.N.  
6/1/05

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800